The invention relates to the radio electronics and may be used for introduction of the programmed phase shift in the signal's way.
Summary of the invention consists in that the phase shifter comprises the first stage (1), provided with a signal input (2), a signal output (3) and a ground connection (4), the stage also comprises two resistors (6, 7), an operational amplifier (5) and a capacitor (8), having one contact connected to the non-inverting input of the operational amplifier, one of the resistors (6) is connected into the circuit of the negative feedback of the operational amplifier, between the inverting input of which and the signal input of the stage it is connected the second resistor (7), and to the output of the operational amplifier is connected the signal output. The first stage comprises additionally a digital-analog converter (9) of code-resistance type, having its output connected between the non-inverting input of the operational amplifier and the ground connection, and the second contact of the capacitor is connected to the signal input of the stage. At the same time, the phase shifter additionally comprises the second and the third stages, having the same structure as the first one, connected in series to the output thereof, as well as a read-only memory unit with $n+m+c$ digital outputs, connected with $n$ outputs to the input of the digital-to-analog converter of the first stage, with $m$ outputs - to the input of the digital-to-analog converter of the second stage and with $c$ outputs - to the input of the digital-to-analog converter of the third stage.
The elements of the first stage provide the control range of the phase shift $\left(0-\varphi_{1}\right)^{0}$, the elements of the second stage $-\left(0-\varphi_{2}\right)^{0}$, and the elements of the third stage $-\left(0-\varphi_{3}\right)^{0}$ so that $\varphi_{1}+\varphi_{2}+\varphi_{3}=360^{\circ}$.
The read-only memory unit comprises a programmed table of digital codes, providing the total linear dependence of the phase shift on the input code of the memory unit and the required phase shift control step.

Claims: 3
Fig.: 1


